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A Low Cost Quadratic Level ECG Compression Algorithm and Its Hardware Optimization for Body Sensor Network System

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***Abstract*— A low cost quadratic level compression algorithm is proposed for body sensor network system. The proposed algorithm reduces the encoding delay and the hardware cost, while maintaining the reconstructed signal quality. The quadratic compression level determined by the mean deviation value is used to preserve the critical information with high compression ratio. The overall CR is 8.4:1, the PRD is 0.897% and the encoding rate is 6.4Mbps. The 16-bit sensor node processor is designed, which supports the proposed compression algorithm. The processor consumes 0.56nJ/bit at 1V supply voltage with 1MHz operating frequency in 0.25-μm CMOS process.**

I. Introduction

Recently, with the increase of the interests about the healthcare, more and more people desire to check their vital signals or health conditions at anytime and anywhere. A body sensor network (BSN) system has been studied to support the continuous healthcare monitoring system. The BSN consists of several sensor nodes and the base station. Fig. 1 shows the flow diagram of the BSN system. The sensor node collects the signal, processes the sensed data, stores and transmits the data. The base station receives, analyzes and diagnoses the gathered data.

The most important requirements for the BSN system are ultra low energy operation for long time battery life and a small footprint for wearability. In general, the highest energy consuming modules are memory and the transmission block [1]. Zigbee and Bluetooth are usually used for the BSN transmission channel [2]. Those wireless communication methods consume a much higher transmitting power than the data processing power. Therefore, minimizing amount of data by data compression is the best way to reduce the total system energy consumption. Many bio signal compression algorithms are introduced [3-6] for medical devices. However, they are concentrated at improvement of compression ratio and the reduction of compression error rate. They didn't consider deeply about the encoding rate, the energy consumption, and the hardware cost.

This paper introduces a quadratic compression level algorithm for low encoding delay and low hardware cost, while maintaining the reconstructed signal quality. Moreover, a hardware design is also proposed, which is optimized to

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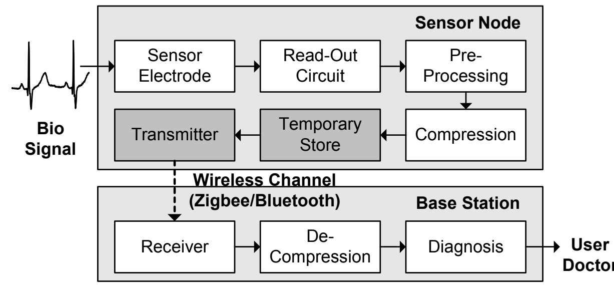

Fig.1. Flow Diagram of Body Sensor Network for Healthcare System

support the proposed algorithm. We verify a low cost design by evaluation of the ECG record data from MIT/BIH databases [7] and implementation of silicon chip.

II. Compression Algorithm

A. Quadratic Compression Level

A lossless and a lossy compression algorithm can be applied to reduce the amount of data. The lossless algorithm doesn't have degree of quantization error which results in a possible loss of diagnostic information. The lossy algorithm has a higher compression ratio, while it has a possibility to miss the significant information. Therefore, a tradeoff is necessary between lossy rate of the critical data and the compression ratio.

Generally, the bio signals are divided into a crucial part and a plain part [8]. For example in the ECG case, the important PQRST complex features are shown in Fig.2. The QRS complex wave is the most important part of the cardiology system to determine arrhythmia [8]. The P and T wave have a high level of information and the remaining parts contain less information [8]. Therefore, in this work, the bio signal is classified into four different level strategies to preserve the property of the information. The main principle of the proposed algorithm is that more bits are assigned to the highest level block, whereas fewer bits are assigned to the lower level block.

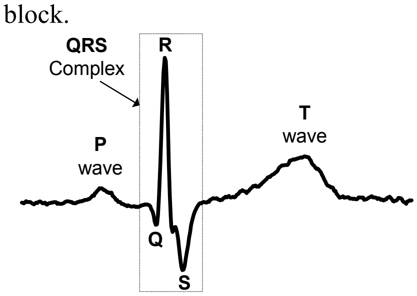

Fig.2. PQRST waves of one beat ECG signal

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In general, the standard deviation (STD) value represents the signal's information [6]. One block with high STD value can have more crucial information. The STD is defined as (1), where, x_i is the sampled bio signal, $\bar{x}$ is the mean value for one block, and N is the block size.

$$STD = \sqrt{\frac{\sum_{i=0}^{N-1}(x_i - \bar{x})^2}{N}} \quad (1)$$

However, the STD requires the complex calculations such as square root ($\sqrt{x}$) and squaring (x^2). Therefore, in this work, the mean deviation (MD) value is proposed to determine the quadratic compression level (QCL) instead of the STD. The MD is defined as:

$$MD = \frac{\sum_{i=0}^{N-1}| x_i - \bar{x} |}{N} \quad (2)$$

The MD requires the only absolute value calculation and it can be consists of smaller hardware than STD. Nevertheless, the MD brings the almost same result as STD as shown in Fig.3(b-c). The average error between STD-QCL and MD-QCL is about 1.6% as shown in Fig.3(d). Table-I compares the performance of the MD with that of STD's, when N is 16. The performance is measured under the conditions of 1MHz operating frequency by using 0.25-µm CMOS technology. The latency and the area of the MD are measured as 18-cycle and 10,000-µm^2, respectively, while those of STD are measured as 42-cycle and 166,000-µm^2, respectively. The 16-bit radix-4 square-root is used for the performance comparison [9]. By using the MD value, the hardware implementation can be much simpler.

After calculation of the MD value, each block is classified into four compression levels by comparing the MD value and the three reference values (ref_0, ref_1, ref_2) as (3), the proposed QCL equation.

$$QCL(CR_{block}) = \begin{cases} 0\,(16:1) & if, MD < ref_0 \\ 1\,(8:1) & if, ref_0 \le MD < ref_1 \\ 2\,(4:1) & if, ref_1 \le MD < ref_2 \\ 3\,(2:1) & if, MD \ge ref_2 \end{cases} \quad (3)$$

The compression ratio of unit block (CR_{block}) is determined according to the QCL. The CR_{block} of 3rd, 2nd, 1st, and 0th level are 2:1, 4:1, 8:1, and 16:1, respectively. If the percentage of each level is P_0:P_1:P_2:P_3 = 60%:25%:10%:5%, the overall compression ratio (CR) is 8.4:1.

TABLE I. COMPARISON RESULTS OF MD WITH STD

	Latency (Cycle)			Area (µm^2)		
	Unit	STD	MD	Unit	STD	MD
MEAN	2	1	1	8k	1	1
SUB	1	16	16	2k	1	1
SQR	1	16	0	32k	1	0
SQRT	8	1	0	84k	1	0
Total		42	18		126k	10k

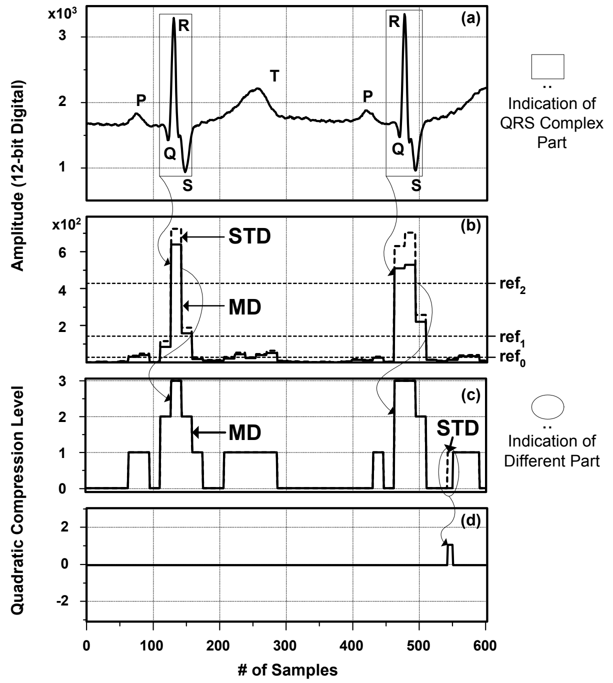

Fig.3.Process of QCL Compression Algorithm (a) Original ECG Signal (b) STD and MD Value (c) Quadratic Compression Level by STD and MD (d) Difference QCL between STD and MD

The ECG data from MIT/BIH is used to verify the efficiency of the proposed algorithm as shown in Fig.3. The sampling rate and the resolution are 360 samples/s and 12 bits, respectively. If the proposed QCL equation is applied to the ECG signal, the QRS complex belongs in 3rd level, Q and S part in 2nd level, P and T part in 1st level, and other parts in 0th level as shown in Fig.3.

B. Reference Value Selection

In order to obtain a high quality of compression, it is important to choose the three reference values (*ref*$_0$, *ref*$_1$, *ref*$_2$). Refer to the above proposed percentage (P_0:P_1:P_2:P_3=60:25:10:5), the reference values can be determined by the statistical graph of MD value as shown in Fig.4. The point of 95% (*ref*$_2$) is about 350, which are the half of maximum MD value (MD_{max}). The points of 85% (*ref*$_1$) and 60% (*ref*$_0$) are 1/8 and 1/16 of the MD_{max}, respectively. The reference values are determined in a real time by shifting the recent MD_{max} value.

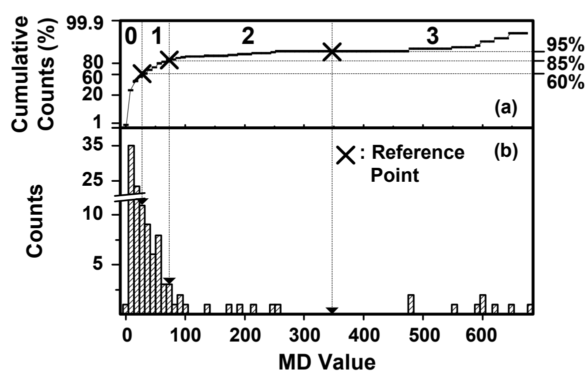

Fig.4. (a) Cumulative Probability Graph (b) Statistical Graph of MD

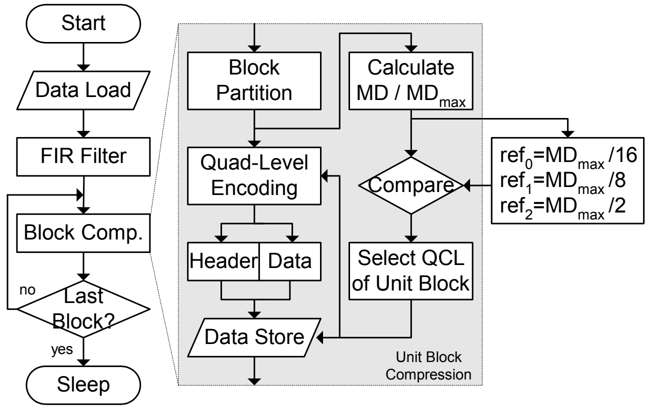

Fig.5. Data Flow Graph of Proposed Quad-Level Compression Algorithm

C. Proposed Compression Algorithm

Fig.5 shows the data flow graph of the proposed QCL algorithm. The detailed algorithm is as follows:

Step 1. Pass the data through a FIR filter to reduce the noise.
Step 2. Partition the data into blocks. In this work, the size a block is 16 words.
Step 3. Calculate the MD value of unit block. And update the MD_{max} and the reference values (ref_0-ref_2).
Step 4. Each block is divided into the four levels by comparing the MD and the reference values. The QCL is updated in real time according to the wave shape.
Step 5. Encode the block into compressed data and header. The CR_{block} of 3rd, 2nd, 1st and 0th level are 2:1, 4:1, 8:1 and 16:1, respectively.
Step 6. Store the result to the data memory.
Step 7. Repeat step1 – step6 until the input data is finished.

When decoding the compressed data, the linear interpolation method is used for a smooth reconstructed waveform and small error rate. Fig.6 shows the example of the QCL compression result. The original signal, encoded signal and the reconstructed signal of the ECG are shown.

III. HARDWARE IMPLEMENTATION

In order to achieve a low cost operation, the optimized hardware design is also necessary as well as the algorithm.

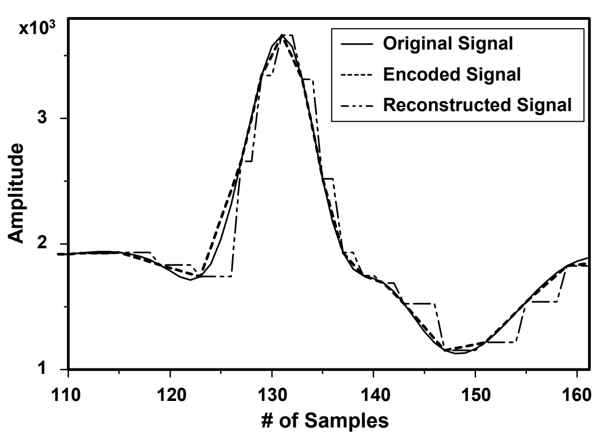

Fig.6. Example of ECG Signal by QCL Compression Algorithm

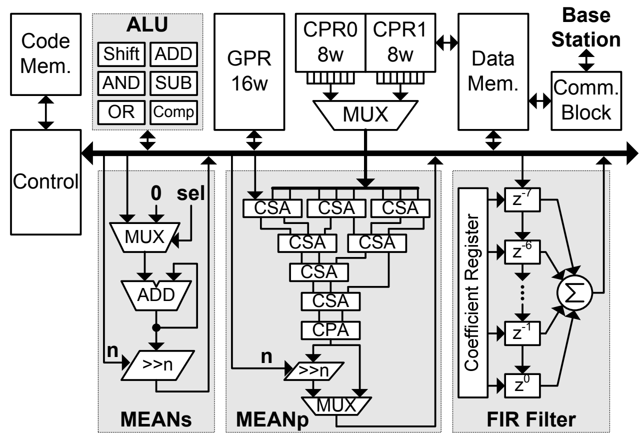

Fig.7. Block Diagram of RISC

In this work, the processor is designed for a sensor node of a body sensor network. The processor is designed in 3 pipeline RISC architecture and Fig.7 shows the block diagram of the top architecture. The processor implements 16-bit Instruction Set Architecture (ISA). 8kB internal SRAMs are integrated for code and data memory. Some special instructions and the datapath are designed for the QCL compression algorithm. The data is moved through the serial mean block (MEANs) and the sum/mean value is calculated. The parallel mean block (MEANp) consists of CSA tree which can calculate the sum/mean value for 9-input at once. The FIR filter consists of 8 tabs and the coefficient registers. The order of the filter can be constructed up to value of 8 with programmable coefficients. The processor has a general purpose register (GPR) and a compression register (CPR0/1). The compression register set (CPR) consists of 16 data register and 4 status register. The level, mean, MD and MD_{max} values are stored in status register. The data is encoded to header and data according to the QCL in the CPR. These unit blocks are connected directly to the register or to the data bus. Those special dedicated unit blocks reduce the operating delay and the code size. After data processing, the processed data is transmitted to base station through the communication block.

With the proposed architecture, the processor is implemented into a chip by using 1-poly 5-metal 0.25μm CMOS technology. Fig.8 shows the chip microphotograph and the size is 2,500 x 1,500 μm^2 with the 8kB SRAM. The energy consumption is 0.56nJ/bit at 1MHz and 1V. Table-II shows the performance summary.

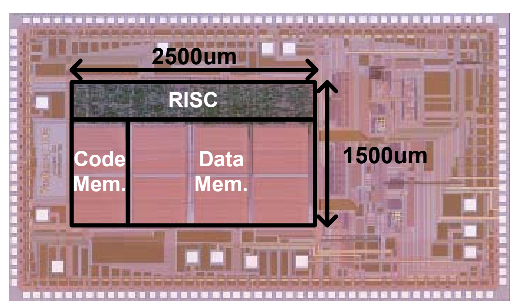

Fig.8. Chip Microphotograph of Processor

TABLE II. PERFORMANCE SUMMARY

Process Technology	1P 5M 0.25μm CMOS
Supply Voltage	1V (Digital) / 2V (Analog)
RISC Frequency	1 – 8MHz
Transmission Rate	1 – 8 Mbps
Memory Capacity	2kB CM / 6kB DM
Energy Consumption	0.56nJ/bit @ 1MHz
Area	15mm^2 (Chip) / 3.75mm^2 (Core)

TABLE III. PERFORMANCE COMPARISON

Algorithm		**CR**	**PRD (%)**	**Encoding Rate**
Hilton [3]	Wavelet (EZW)	8:1	2.6	-
Djohan [4]	Wavelet (DSW)	8:1	3.9	-
Sabarimalai [5]	DFT with DSI	8:1	1.553	-
Kim [6]	WLDECG w/STD	15:1	1.067	2.56kbps
This Work	QL w/MD	8.4:1	0.897	6.4Mbps

IV. RESULTS

The coding performances can be evaluated by the encoding rate, compression ratio (CR) and percentage root mean square difference (PRD). The proposed algorithm takes 40 clock cycles to compress a block (16 words). It can be recalculated to 6.4Mbps with 1MHz operating frequency. The CR_{block} is shown in Fig.9(b). The CR_{block} of dull parts of ECG signal amounts to 16:1, while that of the QRS part is only 3.4:1. The overall CR is 8.4:1.

The error of the proposed compression algorithm is shown in Fig.9(c). The maximum error is 5.8%, however, most of the error is less than 1%. The PRD is usually used to quantify the performance quality of the compression algorithm [6]. The PRD indicates the error between the original ECG samples and the reconstructed data. The PRD is defined as:

$$PRD(\%) = \sqrt{\frac{\sum_{i=1}^{N}(x_i - \tilde{x}_i)^2}{\sum_{i=1}^{N} x_i^2}} \times 100 \qquad (4)$$

where x_i and $\tilde{x}_i$ are the original data and the reconstructed data, respectively. The PRD performance of the proposed algorithm is 0.897. The performance comparison with the

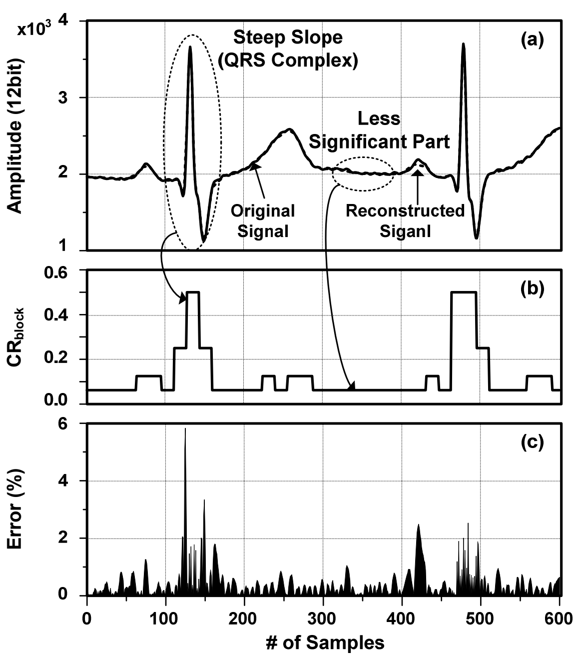

Fig.9. Evaluation Results of QCL Compression Algorithm (a) Original and Reconstructed Signal of ECG (b) Compression Ratio of Unit Block (c) Error Rate between Original and Reconstructed Signal

other works related to the ECG compression is summarized in table-III. The PRD is much smaller than the previous works with similar CR [3-5]. The encoding rate can't be compared because they [3-5] didn't report the encoding rate. So, the encoding rate is compared with Kim's [6]. Kim's work used the STD to classify the compression level. The encoding rate is normalized with 16-word processing. Kim's work has higher CR and similar PRD, however, the encoding rate of 2.56kbps is much lower than this work. As a result, this paper introduces a low cost ECG signal compression algorithm with optimized hardware design. It is suitable to instantaneous and continuous ECG sensor node for body sensor network.

V. CONCLUSION

A low cost quadratic level compression algorithm is proposed to reduce the transmission power consumption and memory capacity for body sensor network system. The proposed algorithm reduces the encoding delay and the hardware cost, while the maintaining reconstructed signal quality. The quadratic compression level by using mean deviation (MD) value is used to preserve the critical information with a high compression ratio. The overall CR is 8.4:1, the PRD is 0.897% and the compression rate is 6.4Mbps. The 16-bit sensor node processor is designed, which is optimized to support the proposed algorithm. The processor consumes 0.56nJ/bit at 1V supply voltage with 1MHz operating frequency in 0.25-μm CMOS process.

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